PCT REQUEST

S00P1411WO00

Original (for **SUBMISSION**)

0 **0-1**	**For receiving Office use only** International Application No.	
0-2	International Filing Date	
0-3	Name of receiving Office and "PCT International Application"	
0-4 0-4-1	**Form - PCT/RO/101 PCT Request** Prepared using	PCT-EASY Version 2.91 (updated 10.10.2000)
0-5	**Petition** The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty	
0-6	**Receiving Office (specified by the applicant)**	Japanese Patent Office (RO/JP)
0-7	**Applicant's or agent's file reference**	S00P1411WO00
I	**Title of invention**	DIGITAL SIGNAL PROCESSING APPARATUS, SYSTEM THEREOF, AND EXTENSION FUNCTION PROVIDING METHOD
II II-1 II-2 II-4 II-5 II-6 II-7 II-8 II-9	**Applicant** This person is: Applicant for Name Address: State of nationality State of residence Telephone No. Facsimile No.	applicant only all designated States except US SONY CORPORATION 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo 141-0001 Japan JP JP 03-5448-2111 03-5448-5709
III-1 III-1-1 III-1-2 III-1-4 III-1-5 III-1-6 III-1-7	**Applicant and/or inventor** This person is: Applicant for Name (LAST, First) Address: State of nationality State of residence	applicant and inventor US only NAKAMURA, Masashi C/O SONY CORPORATION 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo 141-0001 Japan JP JP

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III-2	**Applicant and/or inventor**	
III-2-1	This person is:	Applicant and inventor
III-2-2	Applicant for	US only
III-2-4	Name (LAST, First)	MORIWAKI, Hisayoshi
III-2-5	Address:	C/O SONY CORPORATION 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo 141-0001 Japan
III-2-6	State of nationality	JP
III-2-7	State of residence	JP
III-3	**Applicant and/or inventor**	
III-3-1	This person is:	Applicant and inventor
III-3-2	Applicant for	All designated States except US
III-3-4	Name (LAST, First)	FURUI, Sunao
III-3-5	Address:	C/O SONY CORPORATION 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo 141-0001 Japan
III-3-6	State of nationality	JP
III-3-7	State of residence	JP
III-4	**Applicant and/or inventor**	
III-4-1	This person is:	Applicant and inventor
III-4-2	Applicant for	US only
III-4-4	Name (LAST, First)	HAMADA, Ichiro
III-4-5	Address:	C/O SONY CORPORATION 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo 141-0001 Japan
III-4-6	State of nationality	JP
III-4-7	State of residence	JP
IV-1	**Agent or common representative; or address for correspondence**	
	The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as:	agent
IV-1-1	Name (LAST, First)	SUGIURA, Masatomo
IV-1-2	Address:	7th Floor,Ikebukuro Park Bldg., 49-7,Minami Ikebukuro 2-chome, Toshima-ku, Tokyo 171-0022 Japan
IV-1-3	Telephone No.	03-3980-0339
IV-1-4	Facsimile No.	03-3982-3166
IV-1-5	e-mail	sugipat2@mbc.nifty.com

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V	**Designation of States**	
V-1	Regional Patent (other kinds of protection or treatment, if any, are specified between parentheses after the designation(s) concerned)	AP: GH GM KE LS MW MZ SD SL SZ TZ UG ZW and any other State which is a Contracting State of the Harare Protocol and of the PCT EA: AM AZ BY KG KZ MD RU TJ TM and any other State which is a Contracting State of the Eurasian Patent Convention and of the PCT EP: AT BE CH&LI CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE and any other State which is a Contracting State of the European Patent Convention and of the PCT OA: BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG and any other State which is a member State of OAPI and a Contracting State of the PCT
V-2	National Patent (other kinds of protection or treatment, if any, are specified between parentheses after the designation(s) concerned)	AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH&LI CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
V-5	**Precautionary Designation Statement** In addition to the designations made under items V-1, V-2 and V-3, the applicant also makes under Rule 4.9(b) all designations which would be permitted under the PCT except any designation(s) of the State(s) indicated under item V-6 below. The applicant declares that those additional designations are subject to confirmation and that any designation which is not confirmed before the expiration of 15 months from the priority date is to be regarded as withdrawn by the applicant at the expiration of that time limit.	
V-6	**Exclusion(s) from precautionary designations**	NONE
VI-1	**Priority claim of earlier national application**	
VI-1-1	Filing date	17 November 1999 (17.11.1999)
VI-1-2	Number	Patent Application 11-327161
VI-1-3	Country	JP
VI-2	**Priority document request** The receiving Office is requested to prepare and transmit to the International Bureau a certified copy of the earlier application(s) identified above as item(s):	VI-1

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VII-1	**International Searching Authority Chosen**	Japanese Patent Office (JPO) (ISA/JP)	
VIII	**Check list**	number of sheets	electronic file(s) attached
VIII-1	Request	5	-
VIII-2	Description	24	-
VIII-3	Claims	3	-
VIII-4	Abstract	1	s00p1411_abstract.txt
VIII-5	Drawings	14	-
VIII-7	TOTAL	47	
	Accompanying Items	paper document(s) attached	electronic file(s) attached
VIII-8	Fee calculation sheet	✓	-
VIII-9	Separate signed power of attorney	✓	-
VIII-16	PCT-EASY diskette	-	diskette
VIII-17	Other (specified):	Revenue stamps of transmittal fee and search fee for receiving office	-
VIII-17	Other (specified):	Submission of certificate of payment for international fee	-
VIII-18	**Figure of the drawings which should accompany the abstract**	13	
VIII-19	**Language of filing of the international application**	Japanese	
IX-1	**Signature of applicant or agent**		
IX-1-1	Name (LAST, First)	SUGIURA, Masatomo	

FOR RECEIVING OFFICE USE ONLY

10-1	**Date of actual receipt of the purported international application**	
10-2	**Drawings:**	
10-2-1	Received	
10-2-2	Not received	
10-3	**Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application**	
10-4	**Date of timely receipt of the required corrections under PCT Article 11(2)**	
10-5	**International Searching Authority**	ISA/JP
10-6	**Transmittal of search copy delayed until search fee is paid**	

PCT REQUEST

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Original (for **SUBMISSION**)

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11-1	Date of receipt of the record copy by the International Bureau	

E/P ・ US　　特　許　協　力　条　約

PCT

国際調査報告

（法８条、法施行規則第40、41条）
〔ＰＣＴ１８条、ＰＣＴ規則43、44〕

出願人又は代理人 の書類記号　S00P1411W000	今後の手続きについては、国際調査報告の送付通知様式（ＰＣＴ／ＩＳＡ／２２０）及び下記５を参照すること。	
国際出願番号 ＰＣＴ／ＪＰ００／０８１１３	国際出願日 （日.月.年）　１７．１１．００	優先日 （日.月.年）　１７．１１．９９
出願人（氏名又は名称） ソニー株式会社		

国際調査機関が作成したこの国際調査報告を法施行規則第41条（ＰＣＴ１８条）の規定に従い出願人に送付する。
この写しは国際事務局にも送付される。

この国際調査報告は、全部で　2　ページである。

☐ この調査報告に引用された先行技術文献の写しも添付されている。

１．国際調査報告の基礎

ａ．言語は、下記に示す場合を除くほか、この国際出願がされたものに基づき国際調査を行った。
☐ この国際調査機関に提出された国際出願の翻訳文に基づき国際調査を行った。

ｂ．この国際出願は、ヌクレオチド又はアミノ酸配列を含んでおり、次の配列表に基づき国際調査を行った。
☐ この国際出願に含まれる書面による配列表
☐ この国際出願と共に提出されたフレキシブルディスクによる配列表
☐ 出願後に、この国際調査機関に提出された書面による配列表
☐ 出願後に、この国際調査機関に提出されたフレキシブルディスクによる配列表
☐ 出願後に提出した書面による配列表が出願時における国際出願の開示の範囲を超える事項を含まない旨の陳述書の提出があった。
☐ 書面による配列表に記載した配列とフレキシブルディスクによる配列表に記録した配列が同一である旨の陳述書の提出があった。

２．☐ 請求の範囲の一部の調査ができない（第Ⅰ欄参照）。

３．☐ 発明の単一性が欠如している（第Ⅱ欄参照）。

４．発明の名称は
☒ 出願人が提出したものを承認する。
☐ 次に示すように国際調査機関が作成した。

５．要約は
☒ 出願人が提出したものを承認する。
☐ 第Ⅲ欄に示されているように、法施行規則第47条（ＰＣＴ規則38.2(b)）の規定により国際調査機関が作成した。出願人は、この国際調査報告の発送の日から１カ月以内にこの国際調査機関に意見を提出することができる。

６．要約書とともに公表される図は、
第　2　図とする。☐ 出願人が示したとおりである。　☐ なし
☐ 出願人は図を示さなかった。
☒ 本図は発明の特徴を一層よく表している。

国際調査報告

国際出願番号　ＰＣＴ／ＪＰ００／０８１１３

Ａ．　発明の属する分野の分類（国際特許分類（ＩＰＣ））

Ｉｎｔ．ｃｌ⁷Ｈ０４Ｎ５／４４

Ｂ．　調査を行った分野

調査を行った最小限資料（国際特許分類（ＩＰＣ））

Ｉｎｔ．ｃｌ⁷Ｈ０４Ｎ５／４４　、Ｈ０４Ｌ１２／２８－４６

最小限資料以外の資料で調査を行った分野に含まれるもの
日本国実用新案公報　　１９２２－１９９６
日本国公開実用新案公報１９７１－２００１
日本国登録実用新案公報１９９４－２００１
日本国実用新案登録公報１９９６－２００１

国際調査で使用した電子データベース（データベースの名称、調査に使用した用語）

Ｃ．　関連すると認められる文献

引用文献のカテゴリー＊	引用文献名　及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
Ｙ	ＪＰ，８－７９６４１，Ａ（株式会社東芝）２２．３月．１９９６（２２．０３．９６）、全文　＆ＥＰ，７００２０５，Ａ　＆ＵＳ，５８３８３８３，Ａ	1-12
Ｙ	ＪＰ，５－２８４５２４，Ａ（株式会社東芝）２９．１０月．１９９３（２９．１０．９３）、全文（ファミリーなし）	1-12
Ｙ	ＪＰ，９－５０３１０８，Ａ（ベル・コミュニケーションズ・リサーチ）２５．３月．１９９７（２５．０３．９７）、全文、＆ＥＰ，７４６９２０，Ａ　＆ＵＳ，５６００６４３，Ａ	1-12

☐ Ｃ欄の続きにも文献が列挙されている。　　☐ パテントファミリーに関する別紙を参照。

＊　引用文献のカテゴリー
「Ａ」特に関連のある文献ではなく、一般的技術水準を示すもの
「Ｅ」国際出願日前の出願または特許であるが、国際出願日以後に公表されたもの
「Ｌ」優先権主張に疑義を提起する文献又は他の文献の発行日若しくは他の特別な理由を確立するために引用する文献（理由を付す）
「Ｏ」口頭による開示、使用、展示等に言及する文献
「Ｐ」国際出願日前で、かつ優先権の主張の基礎となる出願の日の後に公表された文献
「Ｔ」国際出願日又は優先日後に公表された文献であって出願と矛盾するものではなく、発明の原理又は理論の理解のために引用するもの
「Ｘ」特に関連のある文献であって、当該文献のみで発明の新規性又は進歩性がないと考えられるもの
「Ｙ」特に関連のある文献であって、当該文献と他の１以上の文献との、当業者にとって自明である組合せによって進歩性がないと考えられるもの
「＆」同一パテントファミリー文献

国際調査を完了した日	国際調査報告の発送日
２９．０１．０１	13.02.01

国際調査機関の名称及びあて先	特許庁審査官（権限のある職員）	５Ｐ	９１８７
日本国特許庁（ＩＳＡ／ＪＰ） 郵便番号１００－８９１５ 東京都千代田区霞が関三丁目４番３号	西谷　憲人　印		
	電話番号　０３－３５８１－１１０１　内線　３５８１		

様式ＰＣＴ／ＩＳＡ／２１０（第２ページ）（１９９８年７月）

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特願平11/327161
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(71) 出願人 (米国を除く全ての指定国について): ソニー株式会社 (SONY CORPORATION) [JP/JP]; 〒141-0001 東京都品川区北品川6丁目7番35号 Tokyo (JP).

(72) 発明者; および
(75) 発明者/出願人 (米国についてのみ): 中村真司 (NAKAMURA, Masashi) [JP/JP]. 森脇久芳 (MORIWAKI, Hisayoshi) [JP/JP]. 古居素直 (FURUI, Sunao) [JP/JP]. 濱田一郎 (HAMADA, Ichiro) [JP/JP]; 〒141-0001 東京都品川区北品川6丁目7番35号 ソニー株式会社内 Tokyo (JP).

(74) 代理人: 杉浦正知(SUGIURA, Masatomo); 〒171-0022 東京都豊島区南池袋2丁目49番7号 池袋パークビル7階 Tokyo (JP).

(81) 指定国 (国内): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

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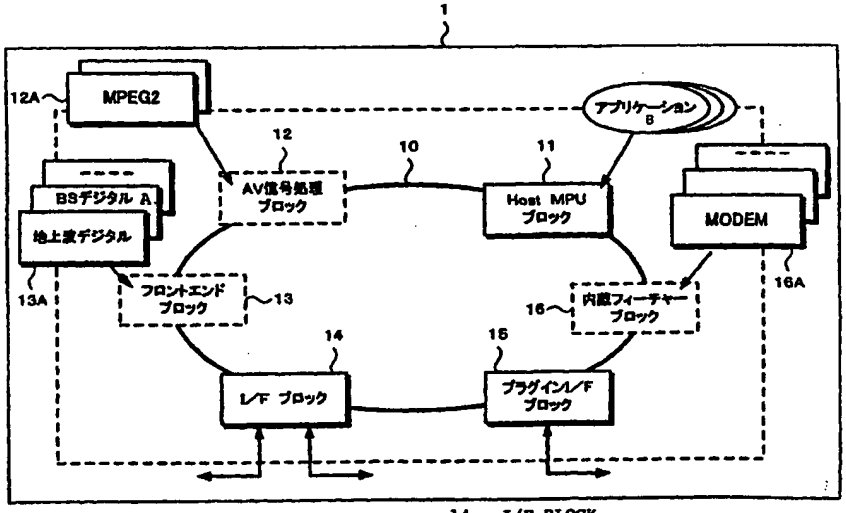
[続葉有]

(54) Title: METHOD AND APPARATUS FOR DIGITAL SIGNAL PROCESSING AND METHOD OF PROVIDING EXTENSION FUNCTION

(54) 発明の名称: ディジタル信号処理装置及びシステム、並びに拡張機能提供方法



11...HOST MPU BLOCK
12...AV SIGNAL PROCESSOR BLOCK
13...FRONT END BLOCK
13A...NORMAL DIGITAL
14...I/F BLOCK
15...PLUG-IN I/F BLOCK
16...BUILT-IN FEATURE BLOCK
A...BS DIGITAL
B...APPLICATION

(57) Abstract: Elements required for a digital television receiver are divided into a plurality of digital signal processor blocks and a host microprocessor block. The blocks are connected by general buses, through which commands and streams of data are transferred to control the operations of the blocks. Plug-in extension cards detachable to the buses are provided for potential new services. The plug-in extension cards include hardware for implementing extended functions and store command scripts for the hardware. When a plug-in extension card is connected to a bus through an interface, command scripts are uploaded to the host microprocessor block that in turn operates the plug-in extension card based on the received command scripts.

[続葉有]

WO 01/37555 A1

DFESCRIPTION

DIGITAL SIGNAL PROCESSING APPARATUS AND METHOD

Technical Field

The present invention relates to a digital signal processing apparatus, a system thereof, and an extension function providing method that are suitable for a digital broadcast receiving device that receives a satellite digital broadcast or a ground wave digital broadcast, in particular, to those that allow the receiving device to be effectively designed, easily design-changed, and easily applied for an added service and an improved function.

Background Art

Analog television broadcasts are becoming changed to digital television broadcasts. So far, digital satellite broadcast services using CS (Communication Satellites) have been started. In addition, digital satellite broadcast services using BS (Broadcasting Satellites) are being prepared. Moreover, digital television broadcasts using ground waves are scheduled to be started.

In digital television broadcasts, since the frequency efficiency is improved, more channels can be assigned than analog television broadcasts. In addition, HDTV (High Definition Television) broadcasts can be easily performed. Moreover, in digital television broadcasts, various services such as bi-

directional service, data delivery service, and video-on-demand that are not available in conventional analog television broadcasts can be accomplished.

A television receiver that receives such a digital television broadcast is conventionally structured as shown in Fig. 1.

In Fig. 1, a received signal is supplied from an input terminal 101 to a tuner circuit 102. In the case of a CS digital broadcast, a signal of 12 GHz band is received by a parabola antenna (not shown). The received signal is converted into a signal of 1 GHz band by a low noise converter disposed in the parabola antenna. The converted signal is supplied to the tuner circuit 102. The tuner circuit 102 selects a carrier frequency signal of a desired channel from the received signal and performs a demodulating process and an error correcting process for the selected signal. As a result, the tuner circuit 102 decodes the selected signal to a transport stream composed of video packets and audio packets.

An output of the tuner circuit 102 is supplied to a demultiplexer 103. The demultiplexer 103 separates the transport stream into video packets and audio packets.

The video packets are supplied to a video decoder 104. The audio packets are supplied to an audio decoder 105. The video decoder 104 performs a

decompressing process for the video packets corresponding to for example the MPEG 2 (Moving Picture Experts Group) system so as to decode the video packets to video data. In addition, the audio decoder 105 performs a decompressing process for the audio packets corresponding to the MPEG system so as to decode the audio packets to audio data.

The video data decoded by the video decoder 104 is supplied to a graphics processing circuit 106. The graphics processing circuit 106 performs a picture process. An output of the graphics processing circuit 106 is output from an output terminal 107. An output of the audio decoder 105 is output from an output terminal 108.

The tuner circuit 102, the demultiplexer 103, the video decoder 104, the audio decoder 105, and the graphics processing circuit 106 are controlled by an MPU (Micro Processor Unit) 111. A bus 111 extends from the MPU 111. The tuner circuit 102, the demultiplexer 103, the video decoder 104, the audio decoder 105, and the graphics processing circuit 106 are connected to the bus 110.

In addition, a modem 112 and for example an IEEE (Institute of Electrical and Electronics Engineers) 1394 interface 113 are connected to the bus 110. The modem 112 is used to perform a charging process. The IEEE 1394 interface 113 exchanges a

stream with an external device.

As was described above, in a conventional receiver for a digital television broadcast, the entire receiver is controlled by an MPU. The MPU centrally controls each portion of hardware using commands thereof in consideration of precise timing levels thereof.

However, in that method of which the MPU centrally controls the entire device in consideration of each portion of the hardware, since the design work should be performed for each device, if the design of the device is changed, software should be largely rewritten and hardware should be largely changed. Thus, the developing efficiency of such a method is low. In addition, since parts cannot be used in common or structured as modules, the cost of the device may rise. In addition, the size of the device may become large. Moreover, digital television broadcasts provide various types of services. Thus, in the method of which the MPU centrally manages the entire device, it is difficult to deal with new services.

Thus, functions necessary for a television receiver may be structured as blocks and connected through a common bus. For conventional television receivers, a standardized controlling bus has been proposed.

However, the conventional controlling bus is

used to exchange control data among the MPU and the individual blocks. Thus, streams of video data and audio data are not sent to the bus. In a digital television broadcast, since streams of video data and audio data should be processed, the conventional bus that exchanges only control data cannot be used.

Although a bus for control data and another bus for streams of video data and audio data may be separately disposed, streams and control data should be synchronized. To do that, a timing signal is required. When the timing signal is sent, the buses depend on hardware. Thus, a general-purpose designing method cannot be used.

On the other hand, in personal computers, there are standardized buses such as PCI (Peripheral Component Interconnect) and ISA (Industry Standard Architecture). Like personal computers, in television receivers for digital television broadcasts, it is likely that a standardized bus is required.

However, in personal computers, when hardware for a new function is connected to a bus, software of a driver for the hardware should be installed. Thus, the user should perform the installing operation for the software.

When a digital television broadcast is processed, streams of video data and audio data that are transferred at high speed should be processed.

However, when a personal computer handles such streams, a high speed CPU and a large capacity memory are required.

Therefore, an object of the present invention is to provide a digital signal processing apparatus and a receiving method that allow the developing efficiency to be improved and the design to be easily changed.

Another object of the present invention is to provide a digital signal processing apparatus and a method that allow a new service and a change of a broadcasting system to be easily handled.

Disclosure of the Invention

The present invention is a digital signal processing apparatus, comprising:

a plurality of digital signal processing blocks and a host arithmetic operation processing block as functions necessary for processing a digital signal; and

a bus for connecting the host arithmetic operation processing block and the plurality of digital signal processing blocks,

wherein commands for controlling the operations of each of the blocks and data of streams are transferred through the bus.

The present invention is a digital signal processing method, comprising the steps of:

structuring functions necessary for

processing a digital signal as a plurality of digital signal processing blocks and a host arithmetic operation processing block; and

connecting the host arithmetic operation processing block and the plurality of digital signal processing blocks through a bus,

wherein commands for controlling the operations of each of the blocks and data of streams are transferred through the bus.

Elements necessary for a digital television receiver are structured as blocks and connected through a general-purpose bus. Thus, by replacing only blocks, various types of digital television broadcasts that differ in carrier waves, modulating systems, and compressing systems can be handled. Thus, the developing efficiency is improved. In addition, when a new service is started, by adding hardware, the service can be easily handled.

Brief Description of Drawings

Fig. 1 is a block diagram showing an example of a conventional receiving device for a digital television broadcast; Fig. 2 is a block diagram for explaining the basic structure of the present invention; Fig. 3 is a schematic diagram for explaining generations of commands and a screen display; Fig. 4 is a schematic diagram for explaining a command sent from a host processor; Fig. 5 is a schematic diagram for

explaining a command sent from the host processor; Fig. 6 is a flow chart for explaining the case that a driver is installed; Fig. 7 is a block diagram showing an example of a television receiver according to the present invention; Fig. 8 is a block diagram showing an example of an encrypting process performed in the television receiver according to the present invention; Fig. 9 is a block diagram showing another example of the encrypting process performed in the television receiver according to the present invention; Fig. 10 is a perspective view for explaining the television receiver according to the present invention; Fig. 11 is a block diagram for explaining the case that an extension plug-in card is attached to the television receiver according to the present invention; Fig. 12 is a schematic diagram for explaining generations of commands and a display screen in the case that a new device is attached; Fig. 13 is a flow chart for explaining the case that the extension plug-in card is attached to the television receiver according to the present invention; and Fig. 14 is a flow chart for explaining the case that the extension plug-in card is attached to the television receiver according to the present invention.

Best Modes for Carrying out the Invention

Next, with reference to the accompanying drawings, an embodiment of the present invention will

be described. According to the embodiment of the present invention, a digital television receiver is structured in such a manner that elements necessary for the digital television receiver are structured as blocks and connected through a bus.

When elements necessary for a digital television receiver are structured as blocks and connected through a bus, various types of digital television broadcasts that vary in carrier waves, modulating systems, and compressing systems can be handled. Thus, the developing efficiency of digital television receivers is improved. In addition, when a new service is started, by adding hardware for the service, the device can easily handle the service.

Fig. 2 shows the basic structure of a digital television receiver of which elements necessary for the receiver are structured as blocks and connected through a bus.

In Fig. 2, a digital television receiver 1 is structured in such a manner that blocks 11, 12, 13, 14, 15, and 16 necessary for the digital television receiver 1 are connected to a bus 10. The blocks 11, 12, 13, 14, 15, and 16 necessary for the digital television receiver are a host MPU block 11, an AV signal processing block 12, a front end block 13, an interface block 14, a plug-in interface block 15, and a built-in feature block 16 that are connected to the bus

10.

The host MPU block 11 controls the entire receiver. The AV signal processing block 12 performs a decompressing process for a video stream and an audio stream and a graphic process. The front end block 13 selects a carrier wave signal of a desired channel from a received television broadcast and performs a demodulating process, an error correcting process, and so forth for the selected signal so as to decode the video stream and the audio stream. The interface block 14 is an interface such as the IEEE 1394 interface for connecting the receiver with an external device. The plug-in interface block 15 is an interface for connecting the receiver with hardware for an extension function. The built-in feature block 16 accomplishes a required built-in function.

Chronological successive streams of video data and audio data, commands, and data are transferred to the bus 10. The commands are high level layer commands that are not on real time basis and that do not depend on hardware structure, not low level layer commands for directly controlling hardware. For example, a command "Receive a frequency of X channel." is issued to the front end block 13. Those commands are also general-purpose script type commands such as "Enlarge (or reduce) the screen." or "Draw a circle." that are issued to the AV signal processing block 12.

When a script is described with hypertext, such operations can be easily accomplished.

In other words, as shown in Fig. 3, a script of which up - down keys 201A and 201B and enlarge - reduce keys 201C and 201D are displayed and commands CMD1 to CMD4 corresponding to the indications 201A to 201E are embedded is created with hypertext. When such a script is displayed, a screen shown in Fig. 3 is displayed on a screen of a browser. When the indications 201A to 201D for the channel up - down buttons and screen enlarge - reduce buttons are clicked, commands CMD1 to CMD4 corresponding thereto are generated. The commands are sent to the relevant blocks 11 to 16. When a block receives such a command, the block performs a process corresponding to the command. To cause each block to perform more complicated process, JAVA or the like can be used.

Of course, the present invention is not limited to the use of hypertext and JAVA.

The physical structure of the bus 10 is standardized. The blocks 11, 12, 13, 14, 15, and 16 are designed so that they comply with the standardized bus. Basic blocks such as the host MPU block 11, the interface block 14, and the plug-in interface block 15 may be disposed on a mother board. The other blocks 12, 13, and 16 may be disposed on a daughter board. The blocks 12, 13, and 16 may be connected to the

standardized bus. Alternatively, the individual blocks 11, 12, 13, 14, 15, and 16 may be structured as integrated circuits or modules.

In the above example, the receiver is divided into the host MPU block 11, the AV signal processing block 12, the front end block 13, the interface block 14, the plug-in interface block 15, and the built-in feature block 16. However, it should be noted that the dividing method is not limited to such an example.

Of course, when each block is disposed on a board, one block is not always composed of one board. In other words, two or more functional blocks may be disposed on one board. For example, the host MPU block 11 and the interface block 14 may be disposed on one board. Of course, one block may be composed of a plurality of boards.

Each of the block 11, 12, 13, 14, 15, and 16 interprets a command received through the bus 10, executes a process corresponding to the command, and processes a stream and data received through the bus 10.

Since a command that does not largely depend on hardware is received through the bus 10, each of the blocks 12, 13, 14, 15, and 16 has a CPU (Central Processing Unit) in many cases so as to interpret the received command and process it. The CPU of each of the blocks 12, 13, 14, 15, and 16 interprets a received command and executes a process corresponding to the

command. Each of the blocks 12, 13, 14, 15, and 16 has a driver that operates hardware corresponding to the received command. A portion that largely depends on hardware completes a process in the block thereof.

In other words, as shown in a conceptual diagram shown in Fig. 4, the host MPU block 11 side has a high level interface HIF for a process with a high level command that is a general purpose command and that does not depend on hardware. On the other hand, each of the blocks 12, 13, 14, and 15 side has a driver DRV that interprets a high level command and performs a process that more depends on hardware and a low level interface LIF that directly controls the hardware.

The host MPU block 11 side sends a high level command through the high level interface HIF and transfers it to each block through the bus 10. The driver DRV of each block interprets a high level command. In that case, portions that depend on hardware are handled by the driver DRV of each of the blocks 12, 13, 14, and 15.

On the other hand, as shown in Fig. 5, the host MPU block 11 side may have a driver DRV. However, in the case shown in Fig. 5, when new hardware is added or hardware is changed, a new driver DRV should be installed or the existing driver DRV should be changed.

High speed streams such as streams of video data and audio data and data that is not on real time

basis such as commands and data are transferred to the bus 10. A bus that can transfer different types of data may have two bands that are a band for a high speed stream such as video data and audio data and a band for data that is not on real time basis such as commands. Alternatively, data may be assigned priority in such a manner that streams of video data and audio data are assigned high priority so that the streams of video data and audio data are transmitted at high speed.

A command that is transmitted to the bus 10 is for example a script type command that is not on real time basis unlike a timing control command. Thus, the data amount of a command that is sent can be remarkably suppressed. Consequently, the same bus 10 can send both commands and streams of video data and audio data.

In such a manner, the digital television receiver is structured in such a manner that the individual blocks 11, 12, 13, 14, 15, and 16 are connected through the bus 10 and commands, streams, and data are exchanged through the bus 10. Thus, the digital television receiver can easily handle various types of television broadcasts. Consequently, the developing environment of the receiver is remarkably improved.

For example, when a ground wave digital broadcast is started, a television receiver that

receives it should be newly developed. However, when the receiver is designed from the beginning as the service the ground wave digital broadcast is started, the developing efficiency of the receiver becomes low.

Although the carrier frequency, modulating system, error correcting system, transport stream structure, and so forth of the conventional digital satellite broadcasts are different from those of ground wave digital broadcasts, when other systems of the conventional digital satellite broadcasts are the same as those of the ground wave digital broadcasts, only the AV signal processing block 12 and the front end block 13 for the ground wave digital broadcasts can be developed. In that case, as the services of the ground wave digital broadcasts are started, an AV signal processing block 12A for ground wave digital broadcasts and a front end block 13A for ground wave digital broadcasts are developed. When only the AV signal processing block 12 and the front end block 13 are substituted with the AV signal processing block 12A and the front end block 13A, respectively, the television receiver can handle the ground wave digital broadcasts that will be newly started. Thus, it is not necessary to develop a receiver for ground wave digital broadcasts from the beginning. Even if particular portions for ground wave digital broadcasts are required, only those portions can be newly developed.

In addition, the operation of the receiver can be changed by changing the application program of the host MPU block 11.

Likewise, receivers for digital television broadcasts through satellites in European countries and receivers for digital television broadcasts of US CATV stations can be easily developed without need to newly design those receivers from the beginning.

In CS digital broadcasts, a television receiver has a modem that is used for a charging process and that is connected to a management company through a telephone line. In such a case, a modem 16A is disposed as the built-in feature 16. Thus, a device necessary for receiving such a broadcast service can be easily mounted as the built-in feature block 16.

In addition, a music data downloading service, a video-on-demand service, and other services are expected. To receive a new service, hardware may be added. In that case, the hardware is added as a device attached to the plug-in interface block 15.

When a block is replaced with another one or when a new device is attached to the plug-in interface block 15, a driver thereof may be required. In such a case, the driver may be stored in a memory of the block or a memory of the device attached to the plug-in interface block 15. When the block is replaced or the device is attached to the plug-in interface block 15,

the driver may be automatically installed. In that case, the operability is improved.

In addition, as shown in Fig. 6, when a block is replaced or when a device is attached to the plug-in interface block 15, a service center may be called and a relevant driver may be downloaded therefrom.

In other words, as shown in Fig. 6, it is determined whether a block has been replaced or a new device has been attached to the plug-in interface block 15 (at step S101). When a block has been replaced or a new device has been attached to the plug-in interface block 15, the replaced device or the new device is recognized (at step S102). Thereafter, the service center is called by a telephone (at step S103). When the service center is called, software of the driver corresponding to the recognized device is transmitted through the telephone line. As a result, the software of the driver is downloaded (at step S104).

Alternatively, software of the driver may be downloaded with a digital satellite broadcast signal or a digital ground wave broadcast signal.

Of course, only when each block requires a driver as shown in Fig. 4, the driver should be installed. Thus, when commands for individual blocks are high layer commands, it is not necessary to install a driver. However, in that case, when software of a portion that depends on hardware is changed, it may be

necessary to install a relevant driver.

As described above, digital television broadcasts are performed through various transmission mediums such as a satellite, a ground wave, a CATV network, and a television line. Carrier waves, modulating systems, and compressing systems used for digital television broadcasts vary depending on transmission mediums, countries and areas, broadcasting companies, and so forth. In addition, in digital television broadcasts, various services such as HDTV broadcast, data delivery service, and video-on-demand service are expected. Thus, receivers for digital television broadcasts corresponding to various transmission mediums, areas, services, and so forth should be developed.

As described above, blocks that accomplish individual functions of a television receiver are connected to a standardized bus. Streams of video data and audio data and commands are exchanged through the standardized bus. In that case, the developing efficiency of television receivers is improved. In addition, various types of television receivers can easily handle services that will be newly started.

Fig. 7 shows an example of the real structure of such a television receiver. In Fig. 7, an internal bus 22 extends from a host MPU 21. A ROM (Read Only Memory) 23 is connected to the bus 22. An additional

logic 24 is connected to the internal bus 22 so as to extend a function.

The ROM 23 stores an application program for operating the entire television receiver. An SDRAM 25 is connected to the host CPU 21. The SDRAM 25 stores user's personal information and various types of setting information. The host CPU 21 is connected to a bus 30 through a bus controller 26.

The bus 30 is used to transmit streams of video data and audio data that are chronologically successive data and commands and data. The commands are high layer commands that do not depend on hardware and that are not on real time basis.

An AV signal processing block 31, a front end block 32, an external interface block 33, and a built-in feature block 34 are connected to the bus 30. In addition, the bus 30 has a plug-in interface 35. An extension plug-in card 36 can be attached to the plug-in interface 35.

A portion composed of the host MPU 21 may be disposed on a mother board. Each of the blocks 31, 32, 33, and 34 may be disposed on a daughter board. The shapes and terminal positions of the mother board and the daughter board may be pre-designated so that the daughter boards of the blocks 31, 32, 33, and 34 may be attached and detached to / from the mother board of the host MPU 21. Alternatively, the blocks 31, 32, 33, and

34 may be structured as blocks or integrated circuits.

Data transferred among the host MPU 21, the blocks 31, 32, 33, and 34, and the extension plug-in card 36 through the bus 30 is managed by the bus controller 26. Alternatively, data may be directly transferred among the blocks 31, 32, 33, and 34 and the extension plug-in card 36 not through the host MPU 21 by the DMA (Direct Memory Access) control.

Data can be transferred from one block to one block. Alternatively, data can be transferred from one block to a plurality of blocks. In other words, data can be broadcast. The broadcast transferring operation can be used when a transport stream received from the front end block 32 is transmitted to the AV signal processing block 31 and the external interface block 33 at the same time so that while a picture is being reproduced, the transport stream can be transmitted to a device connected to the external interface block 33.

The AV signal processing block 31 extracts video packets and audio packets from the transport stream and decompresses the video packets and audio packets to original video data and audio data. The AV signal processing block 31 can perform a picture process for the decoded video data.

The AV signal processing block 31 has a CPU 41, a video decoder 42, an audio decoder 43, a demultiplexer 44, a graphics processing circuit 45, and

a bridge circuit 46. The CPU 41, the video decoder 42, the audio decoder 43, the demultiplexer 44, the graphics processing circuit 45, and the bridge circuit 46 are connected to an in-chip bus 47.

The front end block 32 selects a desired carrier wave signal from the received signal, demodulates the selected carrier wave signal, performs an error correcting process for the demodulated signal, and outputs a transport stream. The front end block 32 has a front end pack 51 and a CPU 52. The front end pack 51 has a mixer circuit, a local oscillating circuit, an intermediate frequency amplifying circuit, a demodulating circuit, an error correcting circuit, and so forth that convert the received signal into an intermediate frequency signal.

The interface block 33 provides an interface with an external device corresponding to for example the IEEE 1394 standard. The external interface block 33 has an interface 61 corresponding to for example the IEEE 1394 standard and a CPU 62.

The built-in feature block 34 is used to provide an addition circuit necessary for receiving a digital broadcast. In a digital broadcast, received data is transferred through a telephone line so as to perform a charging process. To do that, a modem is disposed in the built-in feature block 34. The built-in feature block 34 has a circuit 71 that accomplishes

an additional function (in this case, a modem) and a CPU 72.

The plug-in interface 35 provides an extension function for receiving a new service. The extension plug-in card 36 is attached to the plug-in interface 35. The extension plug-in card 36 has an extension function 81 and a CPU 82. The extension function 81 is composed of software and hardware that accomplish an extension function.

The structure shown in Fig. 7 composes a television receiver 20 that receives for example a digital CS broadcast. In that case, the front end block 32 that performs the QPSK demodulating process, the Viterbi decoding process, and the Reed-Solomon code error correcting process is used. The AV signal processing block 31 that decompresses video packets of transport streams compressed corresponding to the MPEG 2 system and audio packets compressed corresponding to the MPEG system is used.

In a digital CS broadcast, for example, a signal of 12 GHz band is used. A received signal of 12 GHz band transmitted from a satellite is received by a parabola antenna (not shown). The received signal is converted into a signal of around 1 GHz by a low noise converter disposed in the parabola antenna and sent to the front end block 32. The front end block 32 selects a carrier wave signal of a desired channel from the

received signal. The front end block 32 performs the QPSK demodulating process, the Viterbi decoding process, and the Reed-Solomon code error correcting process for the signal so as to decode the received signal to the transport stream.

At that point, the received channel is selected corresponding to a command sent from the host MPU 21 through the bus 30. The host MPU 21 sends a high layer command such as "Receive a frequency of X channel." through the bus 30. The command is sent from the bus 30 to the CPU 52 of the front end block 32. The CPU 52 interprets the command and generates a control signal for designating the received frequency to a desired carrier wave frequency corresponding to the command. In reality, the CPU 52 generates a control signal of the PLL that composes the local oscillator. As a result, the frequency of the received channel is designated.

The front end block 32 outputs a transport stream of packets of video data compressed corresponding to the MPEG 2 system and packets of audio data compressed corresponding to the MPEG system. The transport stream is sent to the AV signal processing block 31 through the bus 30. Thereafter, the transport stream is sent from the AV signal processing block 31 to the demultiplexer 44 through the bridge 46 and the in-chip bus 47. The demultiplexer 44 separates the

transport stream into video packets and audio packets. The video packets are sent to the video decoder 42. The audio packets are sent to the audio decoder 43. The video decoder 42 performs the decompressing process for the video data compressed corresponding to the MPEG 2 system so as to decode the video data. The audio decoder 43 performs the decompressing process for the audio data compressed corresponding to the MPEG audio system so as to decode the audio data. The video data decoded by the video decoder 42 is sent to the graphics processing circuit 45 through the in-chip bus 47. The graphics processing circuit 45 performs the picture process for the video data.

The picture process performed by the graphics processing circuit 45 depends on a command received from the host MPU 21 through the bus 30. A high layer command for example "Reduce (or enlarge) the screen." is sent from the host MPU 21 through the bus 30. The command is sent from the bus 30 to the CPU 41 through the bridge circuit 46. The CPU 41 interprets the command and generates a control signal for reducing / enlarging the screen in the designated size corresponding to the command. In reality, the CPU 41 sends a timing signal for reducing or enlarging the screen and a command for directly controlling hardware to the graphics processing circuit 45 corresponding to the received high layer command.

Thus, in that example, the individual functions necessary for structuring the television receiver 20 are connected as the blocks 31, 32, 33, 34, and 35 to the bus 30. Commands and streams are transferred through the bus 30. When the bus 30 is standardized, the developing efficiency of a television receiver is improved. Thus, a television receiver corresponding to a change of a broadcasting system, a change of a service, or an addition of a service can be easily developed.

However, in that case, since streams composed of video packets and audio packets are directly transferred to the bus 30. Thus, an external device may be connected to the bus 30 so as to extract video packets and audio packets sent through the bus 30 and copy them to the device. When the bus 30 is standardized, there is a risk of which a device that is connected to the bus 30 and that extracts video packets and audio packets sent through the bus 30 is easily accomplished.

To protect contents, as shown in Fig. 8, encryption encoders / decoders 48, 58, 68, 78, and 88 are disposed in the blocks 31, 32, 33, 34, and 35, and the extension plug-in card 36 connected to the bus 30, respectively.

The encryption encoders / decoders 48, 58, 68, 78, and 88 encode streams of video packets and audio

packets transferred from the blocks 31, 32, 33, 34, and 35 through the bus 30. Since streams of video packets and audio packets transferred through the bus 30 are encrypted in such a manner, the contents can be protected.

In that example, to protect contents that flow on the bus 30, the encryption encoders / decoders 48, 58, 68, 78, and 88 are disposed in the blocks 31, 32, 33, and 34, and the extension plug-in card 36, respectively. However, since the blocks 31, 32, 33, and 34 are housed in the set of the receiver, the risk of which contents are leaked out from the blocks 31, 32, 33, and 34 is relatively low. On the other hand, the bus 30 extends from the plug-in interface 35 to the outside. When a device that copies data is connected to the plug-in interface 35 and contents are extracted from the bus 30, the risk of which the contents are leaked out becomes the highest.

To prevent that, as shown in Fig. 9, an encoding encoder / decoder 89 may be disposed in the plug-in interface 35 so that data of contents that flow on the bus 30 is not leaked out from the plug-in interface 35.

In the television receiver 20 according to the present invention, when the extension plug-in card 36 is attached to the external extension bridge 35, a new function can be added so that the receiver can

handle a new service.

In other words, as shown in Fig. 10, in the television receiver 20 structured as described above, a card attaching portion 91 is disposed on the front of the television receiver 20. The extension plug-in card 36 is attached to the card attaching portion 91. When the extension plug-in card 36 is attached to the card attaching portion 91, the extension plug-in card 36 is connected to the bus 30 through the plug-in interface 35.

When the extension plug-in card 36 is connected to the bus 30 through the plug-in interface 35, a function corresponding to a new service can be extended.

To allow the function of the extension plug-in card 36 that is attached to work, controlling software may be required. The controlling software may be provided as a record medium such as a magnetic disk or an optical disc. The user may install the software to the television receiver. However, in that case, the user should spend time for the installing operation.

Thus, to prevent that, as shown in Fig. 11, a script is stored in the memory of the extension plug-in card 36. When the extension plug-in card 36 is attached, the script is uploaded to the main memory of the host MPU 21.

In other words, as shown in a conceptual

diagram shown in Fig. 11, the extension plug-in card 36 has a command script CMD, a command interface CIF, and a driver DRV. When a new extension plug-in card 36 is attached, the host MPU 21 recognizes that the extension plug-in card 36 has been attached. Thereafter, the command script CMD for causing the extension plug-in card 36 to operate is uploaded to the host CPU 21 side. When the command script CMD is uploaded to the host MPU 21 side, the host MPU 21 side can generate a command for causing the extension plug-in card 36 that has been attached to operate.

When the extension plug-in card 36 is operated, a script engine SENG of the host MPU 21 side generates a command. The command is sent to the extension plug-in card 36 through the bus 30. The command interface CIF of the extension plug-in card 36 interprets the command. The driver DRV controls hardware corresponding to the received command.

When the extension plug-in card 36 is a device that records and reproduces a program, as shown in Fig. 12, a script is described as hypertext that embeds CMD 11, CMD 12, CMD 13, CMD 14, and CMD 15 for rewind, stop, play, fast forward, and record commands corresponding to a rewind key 202A, a stop key 202B, a play key 202C, a fast forward key 202D, and a record key 202C, respectively. When such a script is read, a screen as shown in Fig. 12 is displayed by a browser.

When the keys 202A to 202E are clicked, the embedded commands are generated. Corresponding to the commands, the operation of the device is controlled.

Fig. 13 and Fig. 14 are flow charts showing such a process. In Fig. 13, when the extension plug-in card 36 is attached (at step S1), the host MPU 21 determines that the extension plug-in card 36 has been attached (at step S2). Thereafter, the host MPU 21 determines whether or not the attached card is the extension plug-in card 36 (at step S3). When the determined result of the host MPU 21 represents that the attached card is not the extension plug-in card 36, the host MPU 21 outputs an alarm (at step S4).

When the determined result of the host MPU 21 represents that the attached card is the extension plug-in card 36, the command script CMD stored in the extension plug-in card 36 is uploaded (at step S5). When the command script CMD stored in the extension plug-in card 36 is uploaded, the host MPU 21 recognizes a command for the attached extension plug-in card 36 and performs a process for the attached extension plug-in card 36.

In Fig. 14, after the command script has been uploaded, when the user performs an operation for the extension plug-in card 36 (at step S11), the script is checked (at step S12). Thereafter, it is determined whether or not the checked result is correct (at step

S13). When the checked result is not correct, an alarm is output (at step S14). When the checked result is correct, the script engine SENG interprets the script (at step S15) and issues a command (at step S15). The extension plug-in device is operated corresponding to the command (at step S17).

In the above example, the case that the new extension plug-in card 36 is attached was described. Likewise, when a new block is added to the bus 30, a command script for the new block can be uploaded in the same manner.

In the above example, a receiver for a digital broadcast was described. The present invention can be also applied to other devices such as a digital VTR.

According to the present invention, elements necessary for a digital television receiver are structured as blocks and connected through a general-purpose bus. Streams of video data and audio data and commands are transferred to the bus. Thus, by replacing only blocks, various types of digital television broadcasts that differ in carrier waves, modulating systems, and compressing systems can be handled. Consequently, the developing efficiency of a television receiver is improved. In addition, when a new service is started, by adding hardware for the service, the service can be easily handled.

Industrial Applicability

As described above, the present invention is particularly suitable for accomplishing a television receiver that receives various types of digital broadcasts that differ in carrier waves, modulating systems, compressing systems, and so forth.

CLAIMS

1. A digital signal processing apparatus, comprising:

a plurality of digital signal processing blocks and a host arithmetic operation processing block as functions necessary for processing a digital signal; and

a bus for connecting said host arithmetic operation processing block and said plurality of digital signal processing blocks,

wherein commands for controlling the operations of each of the blocks and data of streams are transferred through said bus.

2. The digital signal processing apparatus as set forth in claim 1,

wherein said plurality of digital signal processing blocks include at least a front end block for processing a received signal of a digital broadcast.

3. The digital signal processing apparatus as set forth in claim 1,

wherein said plurality of digital signal processing blocks include at least a signal processing block for decoding data of streams.

4. The digital signal processing apparatus as set forth in claim 1,

wherein said plurality of digital signal processing blocks include means for interpreting a

command received through said bus and executing the command.

5. The digital signal processing apparatus as set forth in claim 1,

wherein the command is a high layer command that does not depend on hardware and that is not on real time basis.

6. The digital signal processing apparatus as set forth in claim 1,

wherein the command is described and embedded in a script of hypertext,

wherein the hypertext is interpreted by a browser and a picture for operating the extension function is displayed, and

wherein a command corresponding to the function is embedded and displayed in the picture for operating the extension function.

7. The digital signal processing apparatus as set forth in claim 1,

wherein the data of streams contains video data and / or audio data.

8. The digital signal processing apparatus as set forth in claim 7,

wherein the video data and / or the audio data has been compressed.

9. The digital signal processing apparatus as set forth in claim 1,

wherein said bus is a general-purpose bus, and

wherein each block connected to said bus can be added or substituted.

10. The digital signal processing apparatus as set forth in claim 9,

wherein when each block connected to said bus is added or substituted, software for operating the added or substituted block is automatically installed.

11. The digital signal processing apparatus as set forth in claim 9,

wherein software for operating the added or substituted block is stored in a memory thereof, and

wherein when the block is added or substituted, the software stored in the memory is installed.

12. The digital signal processing apparatus as set forth in claim 9,

wherein when each block connected to said bus is added or substituted, a service center is accessed through a telephone line, software for operating the added or substituted block is downloaded from the service center through the telephone line, and the downloaded software is installed.

13. A digital signal processing method, comprising the steps of:

structuring functions necessary for

processing a digital signal as a plurality of digital signal processing blocks and a host arithmetic operation processing block; and

connecting the host arithmetic operation processing block and the plurality of digital signal processing blocks through a bus,

wherein commands for controlling the operations of each of the blocks and data of streams are transferred through the bus.

14. The digital signal processing method as set forth in claim 13,

wherein the plurality of digital signal processing blocks include at least a front end block for processing a received signal of a digital broadcast.

15. The digital signal processing method as set forth in claim 13,

wherein the plurality of digital signal processing blocks include at least a signal processing block for decoding data of streams.

16. The digital signal processing method as set forth in claim 13,

wherein the plurality of digital signal processing blocks include a step for interpreting a command received through the bus and executing the command.

17. The digital signal processing method as set forth in claim 13,

wherein the command is a high layer command that does not depend on hardware and that is not on real time basis.

18. The digital signal processing method as set forth in claim 13,

wherein the command is described and embedded in a script of hypertext.

19. The digital signal processing method as set forth in claim 13,

wherein the data of streams contains video data and / or audio data.

20. The digital signal processing method as set forth in claim 19,

wherein the video data and / or the audio data has been compressed.

21. The digital signal processing method as set forth in claim 13,

wherein the bus is a general-purpose bus, and

wherein each block connected to the bus can be added or substituted.

22. The digital signal processing method as set forth in claim 21,

wherein when each block connected to the bus is added or substituted, software for operating the added or substituted block is automatically installed.

23. The digital signal processing method as set forth in claim 21,

wherein software for operating the added or substituted block is stored in a memory thereof, and

wherein when the block is added or substituted, the software stored in the memory is installed.

24. The digital signal processing method as set forth in claim 21,

wherein when each block connected to the bus is added or substituted, a service center is accessed through a telephone line, software for operating the added or substituted block is downloaded from the service center through the telephone line, and the downloaded software is installed.

Abstract

Elements necessary for a digital television receiver are structured as a plurality of digital signal processing blocks and a host operation processing block. The blocks are connected through a general-purpose bus. Command for controlling the operations of the blocks and data of streams are transferred through the bus. Thus, by replacing only blocks, various types of digital television broadcasts that differ in carrier waves, modulating systems, and compressing systems can be handled. Consequently, the developing efficiency of a television receiver is improved. In addition, when a new service is started, by adding hardware for the service, the service can be easily handled.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP00/08113

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H04N5/44

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H04N5/44, H04L12/28-46

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Toroku Jitsuyo Shinan Koho 1994-2001
Kokai Jitsuyo Shinan Koho 1971-2001 Jitsuyo Shinan Toroku Koho 1996-2001

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP, 8-79641, A (Toshiba Corporation), 22 March, 1996 (22.03.96), Full text & EP, 700205, A & US, 5838383, A	1-12
Y	JP, 5-284524, A (Toshiba Corporation), 29 October, 1993 (29.10.93), Full text (Family: none)	1-12
Y	JP, 9-503108, A (Bell Communications Research Inc.), 25 March, 1997 (25.03.97), Full text & EP, 746920, A & US, 5600643, A	1-12

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 January, 2001 (29.01.01)	13 February, 2001 (13.02.01)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)

国際調査報告

国際出願番号　PCT／JP00／08113

A.　発明の属する分野の分類（国際特許分類（IPC））

Int.cl⁷H04N5／44

B.　調査を行った分野

調査を行った最小限資料（国際特許分類（IPC））

Int.cl⁷H04N5／44、H04L12／28－46

最小限資料以外の資料で調査を行った分野に含まれるもの
日本国実用新案公報　1922－1996
日本国公開実用新案公報1971－2001
日本国登録実用新案公報1994－2001
日本国実用新案登録公報1996－2001

国際調査で使用した電子データベース（データベースの名称、調査に使用した用語）

C.　関連すると認められる文献

引用文献のカテゴリー＊	引用文献名　及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
Y	JP,8－79641,A(株式会社東芝)22.3月.1996(22.03.96)、全文　&EP,700205,A　&US,5838383,A	1-12
Y	JP,5－284524,A(株式会社東芝)29.10月.1993(29.10.93)、全文（ファミリーなし）	1-12
Y	JP,9－503108,A(ベル・コミュニケーションズ・リサーチ)25.3月.1997(25.03.97)、全文、&EP,746920,A　&US,5600643,A	1-12

☐ C欄の続きにも文献が列挙されている。　☐ パテントファミリーに関する別紙を参照。

＊　引用文献のカテゴリー
「A」特に関連のある文献ではなく、一般的技術水準を示すもの
「E」国際出願日前の出願または特許であるが、国際出願日以後に公表されたもの
「L」優先権主張に疑義を提起する文献又は他の文献の発行日若しくは他の特別な理由を確立するために引用する文献（理由を付す）
「O」口頭による開示、使用、展示等に言及する文献
「P」国際出願日前で、かつ優先権の主張の基礎となる出願の日の後に公表された文献
「T」国際出願日又は優先日後に公表された文献であって出願と矛盾するものではなく、発明の原理又は理論の理解のために引用するもの
「X」特に関連のある文献であって、当該文献のみで発明の新規性又は進歩性がないと考えられるもの
「Y」特に関連のある文献であって、当該文献と他の1以上の文献との、当業者にとって自明である組合せによって進歩性がないと考えられるもの
「&」同一パテントファミリー文献

国際調査を完了した日　29.01.01	国際調査報告の発送日　13.02.01
国際調査機関の名称及びあて先 日本国特許庁（ISA／JP） 郵便番号100－8915 東京都千代田区霞が関三丁目4番3号	特許庁審査官（権限のある職員）　5P　9187 西谷　憲人　印 電話番号　03－3581－1101　内線　3581

様式PCT／ISA／210（第2ページ）（1998年7月）